of the addressed component). Each of the components **41–44** receives and decodes the address. When the addressed component is ready to receive the information, the addressed component returns a gate signal and its clock to a multiplexor **49** of the buffer **46**. The multiplexor **49** transfers the clock from the addressed component to a counter **51** which controls the transfer of the information to the addressed component **41–44**. In this manner, the information is written to the destination component under control of the destination clock and is immediately available for use by the destination component as in the arrangement shown in FIG. **3**.

The multiplexor **49** illustrated in FIG. **4** is used in order to allow the clock of any one of the components to be used to clock the information into or out of the buffer **46**. The multiplexor **49** includes an AND gate **52**. The AND gate **52** receives input signals from all of the components **41–44**. The input signals to the AND gate **52** are gated clock signals from each of the particular components. To accomplish this, an OR gate **54** is placed to receive the clock from the particular component **41–44** and a gate signal from that component. The gate signal indicates that the component is ready to send or receive information and is analogous to the valid signal sent from the source component in the circuit of FIG. **3**. Normally when a component is not ready to transfer information, the gate signal is high. This high value is transferred by the OR gate **54** to the input of the AND gate **52**. If none of the components are ready to send or receive information either because there is no information to send, none of the components are addressed, or the components are not ready if addressed, then a high value appears on each input to the AND gate **52**. This high value is transferred to the counter. Consequently, no clock signal appearing at an OR gate **54** is transferred to the counter **51** to clock the information out of the buffer **46**. On the other hand, when the gate signal at one of the OR gates **54** goes low, then the clock from the component **41–44** at that OR gate **54** is transferred to the AND gate **52**. Since all of the other inputs to the AND gate **52** are high, the output of the AND gate **52** will reflect the high and low values of the clock from the selected destination component for transfer to the counter **51**. In this manner, any of the components **41–44** may furnish its clock to the buffer **46** to clock information to the source component.

Thus, a plurality of asynchronous components may all be arranged with a simple and rapid synchronization system which allows any one of the components to receive the information from any other source component. The packetizing of information and the use of a broadcast bus to send signals from a source to which a plurality of destinations may synchronize, greatly enhances the speed of a computer system and makes possible the transfer of very large amounts of information.

Although the present invention has been described in terms of a preferred embodiment, it will be appreciated that various modifications and alterations might be made by those skilled in the art without departing from the spirit and scope of the invention. The invention should therefore be measured in terms of the claims which follow.

What is claimed is:

1. A computer system comprising a first component operated in response to timing of a first clock; means for storing information; means for transferring information from the first component to the means for storing information always utilizing the first clock without synchronization to another clock, a second component operated in response to timing of a second clock, the timing of the first clock being independent of the timing of the second clock, means for utilizing the second clock to transfer information without synchronization with the first clock from the means for storing information without transferring other data into said means for storing information whereby the information may be immediately utilized by the second component without need for storage by the second component, said means for utilizing the second clock to transfer information without synchronization with the first clock from said means for storing information comprising means for transferring the information in said means for storing information to the second component under control of the second clock, said means for transferring the information in said means for storing information to the second component under control of the second clock includes means for switching the second clock to the terminals used by the first clock, said means for switching the second clock to the terminals used by the first clock includes a multiplexor, said multiplexor coupled to said first component and said second component, said multiplexor receiving a signal from the second component for furnishing a second clock signal from said second clock to said buffer to transfer data to said second component.

2. A computer system as claimed in claim **1** in which the means for utilizing the clock of the second component to transfer information from the storage of the first component in a condition in which it is synchronized for use by the second component comprises means for providing a signal to the second component to indicate that a prescribed amount of information has been stored in the buffer.

3. A computer system as claimed in claim **1**, in which the means for switching the second clock to the terminals used by the first clock includes means for signaling the multiplexor that the second component is ready to accept the information in the buffer.

4. A computer comprising a plurality of components operated in response to timing of different clocks, means for storing information, means for utilizing the clock of any one of the components to transfer information without synchronization of timing of different clocks between one of the components and the means for storing information, means for signaling any of the components that information stored in the means for storing is to be transferred to that one of the components as a destination component, means for utilizing the clock of the destination component to transfer information from the means for storing information without synchronization of timing of different clocks in a condition in which the information is synchronized for use by the destination component wherein the means for utilizing the clock of any one of the components always utilizes the clock of the component transferring information into said means for storing information, and wherein the timing of the clock of the component from which the information was transferred is independent of the timing of the clock of the destination component, said means for utilizing the clock of the destination component to transfer information from the means for storing information in a condition in which it is synchronized for use by the destination component includes a multiplexor for transferring signals from addressed components to the means for storage, said multiplexor coupled to a first component and a second component, said multiplexor receiving a signal from said second component for furnishing a second clock signal from said second clock to said buffer to transfer data to said second component.

5. A computer as claimed in claim 4 in which the means for signalling another of the components that the information stored in the means for storing is to be transferred to the other of the components comprises means for synchronizing

a signal from the means for signalling any one of the components with the clock of the destination component.

6. A computer system as claimed in claim 4 in which the multiplexor comprises an AND gate, and means for transferring gated clock signals from each of the components as inputs to the AND gate.

7. A computer as claimed in claim 6 in which the means for transferring gated clock signals from each of the components as inputs to the AND gate comprises a plurality of OR gates, each such OR gate connected to receive a clock and a gating signal for transferring the clock from one of the components.

8. A computer system comprising:

a first component;

a first clock coupled to said first component, said first component operated in response to timing of said first clock;

a buffer coupled to said first component, said first component always using said first clock to transfer data from said first component to said buffer without synchronizing said transfer of said data to another clock;

a second component coupled to said buffer;

a second clock coupled to said second component, the timing of said first clock being independent of the timing of said second clock, said second component reading said data from said buffer using said second clock without synchronizing said reading to another clock and without transferring other data into said buffer;

a multiplexor coupled to said first component and said second component, said multiplexor receiving a signal from the second component for furnishing a second clock signal from said second clock to said buffer to transfer data to said second component.

9. A computer system as in claim 8 further comprising:

a third component;

a third clock coupled to said third component, said third component operated in response to timing of said third clock, the timing of said third clock being independent of the timing of said first clock,

wherein said first component uses said first clock to transfer further data from said first component to said buffer without synchronizing said transfer of said further data to another clock, and

wherein said third component transfers said further data from said buffer using said third clock without synchronizing said transfer of said further data to another clock.

10. A computer system as in claim 8 further comprising:

a third component;

a third clock coupled to said third component, said third component operated in response to timing of said third clock the timing of said third clock being independent of the timing of said second clock,

wherein said second component uses said second clock to transfer further data from said second component to said buffer without synchronizing said transfer of said further data to another clock, and

wherein said third component transfers said further data from said buffer using said third clock without synchronizing said transfer of said further data to another clock.

11. A computer system as in claim 8 wherein said data may be immediately utilized by said second component without storing said data in said second component.

12. A computer system as in claim 9 wherein said further data may be immediately utilized by said third component without storing said further data in said third component.

13. A computer system as in claim 8 wherein the transfer of said data into said buffer is controlled entirely by said first component and said first clock.

14. A method for transferring data between a plurality of components in a computer system including a first and a second component, said method comprising:

operating said first component using a first clock having a first timing;

operating said second component using a second clock having a second timing independent of said first timing;

transferring an entire packet of data having a plurality of words from said first component to a buffer always using said first clock without synchronizing any of said plurality of words to another clock;

once said entire packet of data is transferred from said first component to said buffer, signaling said second component that said entire packet of data is ready to be transferred to said second component;

transferring said entire packet of data to said second component using said second clock without transferring other data into said buffer;

furnishing a clock signal to said buffer from a multiplexor, said multiplexor coupled to said first component and said second component, said multiplexor receiving a signal from the second component for furnishing a second clock signal from said second clock to said buffer to transfer data to said second component.

15. A method for transferring data as in claim 14, wherein said computer system comprises a third component and wherein said method further comprises:

operating said third component using a third clock having a third timing independent of said first clock;

transferring a further entire packet of data having a second plurality of words from said first component to said buffer using said first clock without synchronizing any of said second plurality of words to another clock;

once said further packet of data is transferred from said first component to said buffer, signaling said third component that said further entire packet of data is ready to be transferred to said third component;

transferring said further entire packet of data to said third component using said third clock without synchronizing any of said second plurality of words to another clock.

16. A method as in claim 14 wherein said second component uses said entire packet of data immediately without first storing said entire packet of data in said second component.

17. A method as in claim 15 wherein said third component uses said further entire packet of data immediately without first storing said further entire packet of data in said third component.

18. A method as in claim 15 wherein said step of signaling said second component occurs by broadcasting a first signal from said first component to said second and third components, said first signal being synchronized to said second clock, and wherein said step of signaling said third component occurs by broadcasting a second signal from said first component to said second and third components, said second signal being synchronized to said third clock.

19. A computer system as in claim 8 further comprising:

a bus for carrying a first signal, said bus being coupled to said first component and said second component, said

first signal being provided by said first component and being synchronized to said second clock, said first signal being received by said second component and causing said second component to read said data from said buffer.

20. A computer system as in claim **9** further comprising:

a bus for carrying a first signal and a second signal, said bus being coupled to said first, second and third components, wherein said first signal is provided by said first component and is synchronized to said second clock, said first signal being received by said second component and said third component and causing said second component to read said data from said buffer, and wherein said second signal is provided by said first component and is synchronized to said third clock, said second signal being received by said third component and by said second component and causing said third component to read said further data from said buffer.

21. A computer system as in claim **19** wherein said data comprises a plurality of words having a selected number of words and wherein said plurality of words are transferred to said buffer without synchronizing any of said plurality of words to any clock except said first clock and wherein said first signal is received by said second component after all of said plurality of words are transferred to said buffer and wherein all of said plurality of words are transferred to said second component from said buffer after said second component receives said first signal.

22. A computer system as in claim **20** wherein said data comprises a plurality of words having a selected number of words, and wherein said plurality of words are transferred to said buffer without synchronizing any of said plurality of words to any clock except said first clock and wherein said first signal is received by said second component after all of said plurality of words are transferred to said buffer, and wherein all of said plurality of words are transferred to said second component from said buffer after said second component receives said first signal, and wherein said further data comprises a further plurality of words, and wherein said further plurality of words are transferred to said buffer without synchronizing any of said further plurality of words to any clock except said first clock and wherein said second signal is received by said third component after all of said further plurality of words are transferred to said buffer and wherein all of said further plurality of words are transferred to said third component from said buffer after said third component receives said second signal.

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